REMARKS

Claims 1-10 are pending. Claims 1-3 and 6-8 are currently amended.

Independent claims 1-2 and 6-7 were rejected as anticipated by Tashiro (U.S. Patent No. 5,042,147). Dependent claims 3-5 and 8-10 were rejected as unpatentable over Tashiro in view of Kado et al. (U.S. Patent App. No. 2004/0164385).

Claims 1-2 and 6-7 have been currently amended and recite a method of manufacturing a mounting substrate or a circuit device in which a plurality of electrodes formed on the mounting substrate are directly electrically interconnected to adjacent electrodes via plating wires. For example, FIGS. 1B, 2B and 4B show a matrix of electrodes 15 formed on the back face of mounting substrate 11 that are *directly* connected to adjacent electrodes via plating wires 11 which provide an *electrical* connection (page 8, lines 10-11, page 9, lines 5-6). Providing direct interconnections to each adjacent back face electrode 15 facilitates electrically connecting the electrodes located in the inner regions of the matrix to those located on the outer regions without having to form plating wires in-between the electrodes. Subsequently, the density of back face electrodes may be increased.

In contrast, the Tashiro patent does not disclose or suggest electrodes formed on a mounting substrate which are *directly interconnected* with each other via plating wires. The Tashiro patent discloses a method of preparing a surface-mounted wiring board 5 in which die pads 1 and bonding pads 2 are arranged on a face of the wiring board 5. The die pads 1 and bonding pads 2 are electrically interconnected using a fine-line pattern (*see* FIG.1, col. 3, lines 21-23). A gold plating film is formed on the die pads 1 and bonding pads 2 using Au-electroplating (col. 3, lines 37-45). A groove is then formed in the wiring board 5 to separate the fine-line pattern that electrically interconnects the die pads 1 and bonding pads 2 (col. 3, lines 46-49).

While the bonding pads 2 of Tashiro are electrically interconnected, they are not directly interconnected. Instead, as FIG. 1 clearly shows, the bonding pads 2 are *indirectly* connected through the use of die pad 1.

The Kado et al. reference discloses a multi-chip module in which a plurality of electrode pads 10 are arranged in an array form on the lower surface of a package substrate 1. The electrode pads 10 are electrically connected to Au bumps 4 formed on the main surface of chips 2A and 2B through wiring lines 5 located on the upper and lower surface and interior of the package substrate 1 (par. 73, 75, 77). An individual multi-chip module is obtained by dicing a multi-wiring substrate 100 in a lattice shape along dicing lines L as shown in FIGS. 4 and 5 (par. 80-81). The Kado et al. reference does not, however, disclose or suggest the electrode pads are directly electrically interconnected with each other via plating wires.

For at least the foregoing reasons, claims 1-2 and 6-7 should be allowed.

Claims 3-5 and 8-10 depend, respectively, from claims 1-2 and 6-7 and should be allowed for the same reason.

Moreover, the dependent claims recite additional features that make these claims independently patentable. For example, claims 3 and 8 recite forming front face electrodes on the front face of a mounting substrate and back face electrodes on the back surface of a mounting substrate. The Office action alleges it would have been obvious to one of ordinary skill in the art to incorporate the back electrode pads 10 and solder bumps 11 disclosed in the Kado et al. reference with the wiring board disclosed in the Tashiro patent in order to obtain the features recited in claims 3 and 8 (Office action, page 4). Applicants respectfully disagree.

Kado et al. discloses the solder bumps 11, which are connected to electrode pads 10, "constitute *external connecting terminals* of the multi-chip module" (par. 0077). Tashiro, however, clearly discloses that the multilayer wiring board is entirely covered by a coating resin (see FIG. 2, col. 4, lines 7-9). Subsequently, if electrode pads 10 and solder bumps 11 of Kado et al. were incorporated on the back surface of the multilayer wiring board of Tashiro, it would not be possible to provide electrical connection externally to the electrode/bumps due to the covering resin.

For this additional reason, claims 3 and 8 should be allowed.

Furthermore, claims 5 and 10 recite cutting off the plating wires by dicing. The Office action alleges it would have been obvious to one of ordinary skill in the art to modify the method of forming a groove as disclosed by Tashiro so that the fine-line patterns are cut by dicing, as disclosed by Kado et al. Applicants respectfully disagree.

In the Kado et al. patent, dicing is used to separate the multi-wiring substrate 100 into multiple package substrates 1 (par. 0081) i.e. the process of dicing forms entirely separate package substrates 1 from the original multi-wiring substrate 100. In the Tashiro patent, however, the groove does not separate the wiring board 5. Instead, the groove is formed only 0.5 mm deep into the wiring board 5 (col. 3, lines 45-51). If the process of dicing was used to cut the fine-line pattern 3, then the SOP-LSI, QFP-LSI, resistor chips, capacitor chips and bonding pads would no longer be located on the same device substrate and the device would be damaged. Therefore, it would not have been obvious to one of ordinary skill in the art to use dicing as disclosed in Kado et al. for the purpose of cutting the fine-line patterns of Tashiro.

For this additional reason, claims 5 and 10 should be allowed.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Conclusion

In view of the above remarks, all remaining claims are allowable and a notice of allowance should be issued.

No fee is believed due. However, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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